CLAIMS

What is claimed is:

1. An apparatus comprising:

a first differential output driver to provide a single ended output voltage in response to an input voltage;

a second differential output driver to provide a single ended output in response to the input voltage, the first output voltage and the second output voltage representative of the positive and inverted input voltage; and

a feedback circuit to monitor the first and second output voltages and apply a bias voltage to at least one of the first and second output drivers to vary the point where the first and second output voltages cross-over as the input voltage changes from a first to a second level.

2. The apparatus of claim 1, wherein the correcting bias voltage forces the first and second output voltages to cross-over at a point substantially equidistant between maximum and minimum output voltages of the first and second differential drivers.

3. The apparatus of claim 1, wherein the first and second output drivers are connected to provide positive and negative outputs to positive and negative conductors of a transmission cable.

4. The apparatus of claim 2, wherein the feedback circuit further includes at least one capacitor, and wherein the feedback circuit places a charge proportional to a difference between an actual cross-over voltage of the first and second output drivers and the equidistant cross-over voltage onto the capacitor to convert the charge into the correcting voltage.

5. The apparatus of claim 4, wherein the at least one capacitor includes a first and second capacitor, wherein the feedback circuit places a charge proportional to a difference between the actual cross-over voltage and the equidistant cross-over voltage onto the first and second capacitors, and wherein the first capacitor supplies a correcting voltage to at least one pull-up bias circuit in the output drivers, and the second capacitor supplies a correcting voltage to at least one pull down bias circuit in the output drivers.

6. The apparatus of claim 5, wherein the feedback circuit applies the correcting voltage to increase a drive strength of the pull-up bias circuit and/or to decrease a drive strength of the pull-down bias circuit if the actual cross-over voltage is lower than the equidistant cross-over voltage.

7. The apparatus of claim 5, wherein the feedback circuit applies the correcting voltage to decrease a drive strength of the pull-up bias circuit and/or to increase the pull-down bias circuit if the cross-over voltage is higher than the equidistant cross-over voltage.

8. The apparatus of claim 4, wherein the first capacitor provides a correcting voltage to a gate of a PMOS transistor in the pull-up bias circuit, and wherein the second capacitor provides a correcting voltage to a gate of an NMOS transistor in the pull-down bias circuit.

9. The apparatus of claim 5, further including:

a differential receiver for detecting a cross-over voltage transition on the differential interface, the differential receiver having a first output;

a single-ended receiver for detecting rail-to-rail transitions on the positive conductor, the receiver for the positive conductor having a second output;

a single-ended receiver for detecting rail-to-rail transitions on the negative conductor, the receiver for the negative conductor having a third output; and

wherein if the cross-over voltage is lower than the equidistant voltage, charge on the first capacitor is reduced while the first output is high and the second output is low and/or charge on the second capacitor is reduced while the first output is low and the third output is low.

10. The apparatus of claim 9,

wherein if the cross-over voltage is higher than the equidistant voltage, charge on the first capacitor is increased while the first output is low and the second output is high and/or charge on the second capacitor is increased while the first output is high and the third output is high.

11. The apparatus of claim 9, wherein the outputs enable switches to apply a high voltage level to the first and second capacitors to increase the charge, and to apply a low voltage level to the first and second capacitors to reduce the charge.

12. The apparatus of claim 11, wherein the switches include transmission-gate switches.

13. The apparatus of claim 1, wherein the transceiver circuit is an interface to a universal serial bus (USB).

14. A method comprising:

measuring a difference between a voltage at which output voltage signals of first and second drivers of a differential signal transceiver cross-over and a voltage point substantially equidistant between maximum and minimum output voltages;

providing a correcting bias voltage proportional to a difference between the cross-over voltage and the equidistant voltage; and

applying the correcting bias voltage to the differential drivers to vary the voltage point where the first and second output voltages cross-over.

15. The method of claim 14, wherein providing a correcting bias voltage includes:

producing a net charge on at least one capacitor in proportion to the difference between the cross-over voltage and the equidistant voltage; and converting the charge into a correcting bias voltage.

16. The method of claim 14, wherein applying the correcting bias voltage to the differential drivers includes feeding back the correcting voltage to the drivers to adjust a drive strength of pull-up and pull-down bias circuits.

17. The method of claim 16, wherein adjusting the drive strength of pull-up and pull-down circuit biasing includes:

increasing the drive strength of the pull-up bias circuit and/or decreasing the drive strength of the pull-down bias circuit if the cross-over voltage is lower than the equidistant voltage; and

decreasing the drive strength of the pull-up bias circuit and/or increasing the drive strength of the pull-down bias circuit if the cross-over voltage is higher than the equidistant voltage.

18. The method of claim 17, wherein

increasing the drive strength of the pull-up bias circuit includes decreasing a gate voltage on a PMOS transistor,

decreasing the drive strength of the pull-up bias circuit includes increasing a gate voltage of the PMOS transistor,

increasing a drive strength of the pull-down bias circuit includes increasing a gate voltage on an NMOS transistor, and

decreasing the drive strength of the pull-down bias circuit includes decreasing a gate voltage on the NMOS transistor.

19. The method of claim 15, wherein the net charge produced is zero when the cross-over voltage matches the equidistant voltage.

20. The method of claim 15, wherein the at least one capacitor includes a first and second capacitor and producing a charge on a capacitor includes switching a power supply rail onto the first and second capacitor.

21. The method of claim 20, wherein adjusting a pull-up circuit bias includes applying a correcting voltage on the first capacitor to adjust a pull-up bias voltage, and adjusting a pull-down circuit bias includes applying a correcting voltage on the second capacitor to adjust a pull-down capacitor voltage.

22. The method of claim 15, wherein measuring further includes:

measuring a cross-over transition on positive and negative conductors of a transmission cable with the differential signal transceiver;

measuring a rail-to-rail transition on the positive conductor of the transmission cable;

measuring a rail-to-rail transition on the negative conductor of the transmission cable; and

wherein producing a net charge includes switching a charge onto the capacitor when there is a mismatch in transition times.

23. The method of claim 22, wherein measuring further includes:

providing a single ended output transition on a differential receiver in response to the cross-over transition;

providing a single ended output transition on an output of a first single ended receiver in response to a transition exceeding a first voltage threshold on the positive conductor; and

providing a single ended output transition on an output of a second single ended receiver in response to a transition exceeding a second voltage threshold on the negative conductor.

24. The method of claim 23, wherein providing the single ended output transition of the differential receiver includes providing a transition that follows the transition on the positive conductor, and wherein switching includes:

a) switching a low supply onto the first capacitor while an output of the differential receiver is at a high voltage and an output of the first single-ended receiver is at a low voltage;

b) switching a high supply onto the first capacitor while the output of the differential receiver is at a low voltage and the output of the first single-ended receiver is at a high voltage;

c) switching a low supply onto the second capacitor while the output of the differential receiver is at a low voltage and an output of the second single-ended receiver is at a low voltage; and

d) switching a high supply onto the second capacitor while the output of the differential receiver is at a high voltage and the output of the second single-ended receiver is at a high voltage.

25. A system comprising:

a transceiver interface coupled to a differential communication bus, the transceiver interface having a differential cross-over voltage of a magnitude between high and low transceiver output voltages;

a transceiver controller in communication with the transceiver interface; and

a cross-over lock feedback circuit to correct deviations of the cross-over voltage from a voltage point equidistant between maximum and minimum output voltages of the transceiver.

26. The system of claim 25, wherein the transceiver interface further includes at least one transceiver driver coupled to the cross-over lock feedback circuit, the driver having pull-up and pull-down circuits; and wherein the feedback circuit feeds back a correcting voltage to the driver to adjust the pull-up and/or pull-down of the driver to correct the cross-over voltage.

27. The system of claim 26, wherein the cross-over lock feedback circuit produces a charge in proportion to a difference of the cross-over voltage from the equidistant voltage to provide the correcting voltage.

28. The system of claim 27, wherein the transceiver interface further includes:

a differential receiver;

a single-ended receiver coupled to a positive node on the differential bus; and

a single-ended receiver coupled to a negative node on the differential bus,

wherein the feedback circuit produces a charge based on asymmetry of switching times at receiver outputs when the cross-over voltage is different from the midpoint voltage.

29. A system comprising:

a transceiver interface coupled to a differential communication bus, the transceiver interface having a differential cross-over voltage of a magnitude between high and low transceiver output voltages;

a transceiver controller in communication with the transceiver interface; and

a cross-over lock feedback circuit to correct deviations of the cross-over voltage from a voltage point equidistant between maximum and minimum output voltages of the transceiver;

a processor in communication with the transceiver controller; and

a DRAM memory in communication with the processor.

30. The system of claim 29, wherein the transceiver interface further includes at least one transceiver driver coupled to the cross-over lock feedback circuit, the driver having pull-up and pull-down circuits; and wherein the feedback circuit feeds back a correcting voltage to the driver to adjust the pull-up and/or pull-down of the driver to correct the cross-over voltage.

31. The system of claim 30, wherein the cross-over lock feedback circuit produces a charge in proportion to a difference of the cross-over voltage from the equidistant voltage to provide the correcting voltage.